

**In the Claims:**

1. (Original) A method for synthesizing an integrated circuit design, the method comprising:

performing physical optimization of block and wire placement, before performing logic synthesis;

partitioning the blocks into cores and shells;

synthesizing the shells and cores; and

recombining the cores and shells into blocks.

2. (Original) The method of Claim 1, wherein performing physical optimization of block placement comprises estimating an area of each block.

3. (Original) The method of Claim 2, wherein performing physical optimization of wire placement comprises determining a pin assignment layout.

4. (Original) The method of Claim 3, wherein performing physical optimization of wire placement further comprises selecting a layer for each wire based on wire length.

5. (Original) The method of Claim 4, wherein performing physical optimization of wire placement further comprises minimizing a delay in each wire by inserting buffers at optimal distances.

6. (Original) The method of Claim 5, wherein synthesizing the shells comprises determining a proportion of time to assign to each shell on each side of a wire.

7. (Original) The method of Claim 5, wherein after synthesizing the shells, the process of performing physical optimization of blocks and wires and partitioning the blocks is incrementally repeated if the wire delays are too long for shell synthesis.

8. (Original) A method for designing deep sub-micron integrated circuits, the method comprising:

performing layout of physical blocks by estimating an area for each block;  
connecting pins of the blocks with no timing constraints;  
assigning each wire to a metal layer pair;  
optimizing the speed of each wire for its respective layer;  
partitioning the blocks into cores and shells;  
synthesizing the shells;  
synthesizing the cores; and  
recombining the shells and cores.

9. (Original) The method of Claim 8, wherein each wire is assigned to a metal layer based on a relative length of the wire.

10. (Original) The method of Claim 9, wherein optimizing the speed of each wire comprises minimizing a delay in each wire by inserting buffers at optimal distances.

11. (Original) The method of Claim 10, wherein synthesizing the shells comprises determining a proportion of time to assign to each shell on each side of a wire.

12. (Original) The method of Claim 11, wherein after synthesizing the shells, the layout procedure is incrementally repeated if the wire delays are too long for shell synthesis.

13. (Original) A method for reducing design cycle time for integrated circuits, the method comprising:

laying out blocks by estimating an area for each block;  
minimizing a delay in each global wire;  
partitioning each block into a core and a shell;  
performing logic synthesis on each shell by utilizing a known delay for each wire;  
performing logic synthesis on each core; and  
recombining the shells and cores.

14. (Original) The method of Claim 13, wherein minimizing a delay in each global wire comprises assigning each wire to a layer, and inserting buffers at optimal distances.

15. (Original) The method of Claim 14, wherein performing logic synthesis on each shell comprises determining a proportion of time to assign to each shell on each side of a wire.

16. (Original) The method of Claim 15, wherein after synthesizing the shells, the layout procedure is incrementally repeated if the wire delays are too long for shell synthesis.

17. (Amended) [[A]] The method according to Claim 1, wherein the method is codified as instructions on a computer readable media, having

~~instructions stored thereon~~ that, when loaded into a computer, cause the computer to perform the steps of the method [[:]]

~~performing physical optimization of block and wire placement, before performing logic synthesis;~~

~~partitioning the blocks into cores and shells;~~

~~synthesizing the shells and cores; and~~

~~recombining the cores and shells into blocks.~~

18-23. (Cancel)

24. (New) A method for synthesizing an integrated circuit design, the method comprising:

performing physical optimization of block and wire placement, before performing logic synthesis;

partitioning the blocks into cores and shells;

synthesizing the shells and cores; and

recombining the cores and shells into blocks;

wherein:

performing physical optimization of wire placement comprises determining a pin assignment layout;

performing physical optimization of wire placement further comprises selecting a layer for each wire based on wire length;

performing physical optimization of wire placement further comprises minimizing a delay in each wire by inserting buffers at optimal distances;

each wire is overdesigned in that it is designed to be as fast as possible at the earliest stages of design and wire changes related to wire speed in subsequent design stages comprise area recovery by dropping repeaters that are not absolutely necessary; and

synthesizing the shells comprises determining a proportion of time to assign to each shell on each side of a wire.

25. (New) The method according to Claim 24, wherein the step of performing physical optimization of block and wire placement is performed without concern for wire delays.

26. (New) The method according to Claim 24, wherein the only estimation utilized in the method is a block size estimation, and the block size is adjusted and the method is re-iterated based on the adjusted block size.

27. (New) The method according to Claim 24, further comprising the steps of connecting pins without timing constraints, and assigning layers to wires qualitatively based on wirelength without regard to timing.

28. (New) The method according to Claim 24, wherein the entire design process is performed without iterations due to timing constraints of any wires.

29. (New) The method according to Claim 24, wherein wire changes related to wire speed in subsequent design stages comprise one of changing layers of the wires and area recovery performed by dropping buffers that are not absolutely necessary.